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Nanoelectronic Programmable Synapses Based on Phase Change Materials for Brain-Inspired Computing

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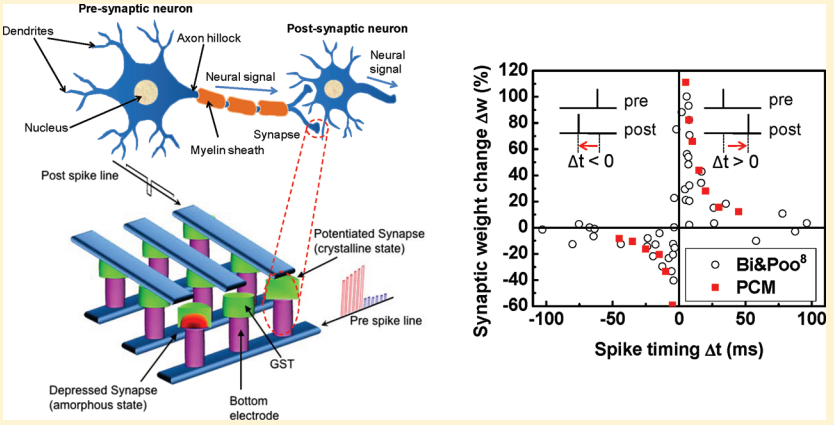
Supporting Information

ABSTRACT:



Brain-inspired computing is an emerging field, which aims to extend the capabilities of information technology beyond digital logic. A compact nanoscale device, emulating biological synapses, is needed as the building block for brain-like computational systems. Here, we report a new nanoscale electronic synapse based on technologically mature phase change materials employed in optical data storage and nonvolatile memory applications. We utilize continuous resistance transitions in phase change materials to mimic the analog nature of biological synapses, enabling the implementation of a synaptic learning rule. We demonstrate different forms of spike-timing-dependent plasticity using the same nanoscale synapse with picojoule level energy consumption.

KEYWORDS: Brain-inspired computing, nanoelectronics, phase change materials, spike timing dependent plasticity, synapse

The efficiency of today's information processors has been dominated by complementary metal−oxide−semiconductor (CMOS) transistor scaling based on Moore's law. However, in the nano era CMOS scaling started to face significant barriers in achieving historical performance gains.[1] Besides the physical limits, the conventional computing paradigm based on binary logic and Von Neumann architecture becomes increasingly inefficient as the complexity of computation increases. For some computational problems (such as genetics data from DNA microarrays, image and sensor data from satellites, relationships in social networks, and metabolic pathways in biological networks) the computation time scales exponentially with the input size,[2] making it difficult to perform such tasks with conventional computers. Hence, new computational paradigms and architectures are being explored to extend the capabilities of information technology beyond digital logic. As compared to biological systems, today's programmable computers are 6 to 9 orders of magnitude less efficient in complex environments.[3] Simulating 5 seconds of brain activity takes 500 s and needs 1.4 MW of power, when state-of-the-art supercomputers (i.e., IBM Blue Gene) are used.[4] The power dissipation in the human central nervous system is on the order of 10 W. The superior features of the brain, lacking in today's computational systems, are ultrahigh density, low energy consumption, parallelism, robustness, plasticity, and fault-tolerant operation. The human brain consists of $\sim 10^{11}$ neurons and an extremely large number of synapses, $\sim 10^{15}$, which act as a highly complex interconnection scheme among neurons.[5] Synapses dominate the architecture of the brain and are responsible for massive parallelism, structural plasticity, and robustness of the brain. They are also crucial to biological computations that underlie perception and learning.[6] Therefore, a compact nanoelectronic device emulating the functions and plasticity of biological synapses will be the most important building block of brain-inspired computational systems.

The anatomical discoveries and physiological studies in the twentieth century have led to the theory that learning could be a consequence of changes in the synaptic strength. The well-known theory based on synaptic plasticity, known as Hebbian learning,[7] suggests that the connection strength between

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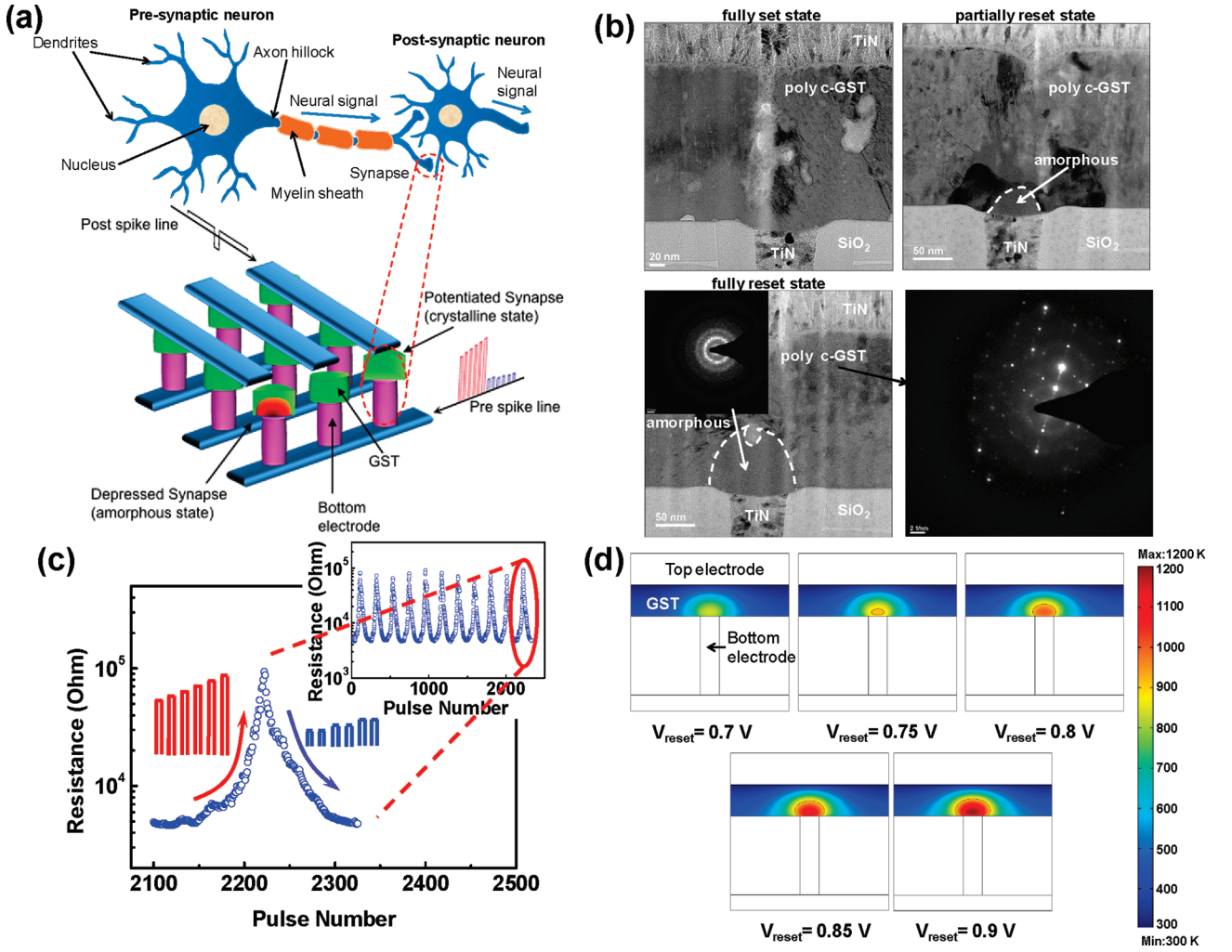

Figure 1. Illustration and characteristics of bioinspired electronic synapses. (a) Interconnection scheme of PCM synapses to reach ultrahigh density and compactness of brain is shown. In the crossbar array architecture, PCM synapses lie between postspike and prespike electrodes, inspired by biological synapses formed between presynaptic and postsynaptic neurons. The cross sections of depressed (mushroom shaped amorphous region shown in red) and potentiated synapses are shown in the schematic. (b) Cross-section TEM images of electronic synapses made of GST are shown. The cells are programmed to fully set (500 Ω), partially reset (200 kΩ), and fully reset states (2 MΩ) before TEM sample preparation. In transition from set state to reset state, volume of the amorphous region at the top of the bottom electrode grows and when it fully covers the bottom electrode, the fully reset state is reached. The inset of the fully reset state shows a diffraction pattern for the mushroom shaped amorphous region. Diffraction pattern away from bottom electrode shows that GST is polycrystalline. (c) Gradual reset of the cell resistance is implemented by using pulses with increasing amplitude in 2−4 V range with 20 mV voltage steps. Gradual set of the cell resistance is achieved by using stair-case pulses with an increasing step of 0.1 V. There are 20 pulses for each voltage step, 0.5, 0.6, 0.7, 0.8, and 0.9 V. (d) Finite element simulations performed with COMSOL are shown. Different colors represent the temperatures across the GST region for reset voltages ranging from 0.7 to 0.9 V. The regions, where $T > 900$ K, are mapped using a solid black line. The region within this line would turn into an amorphous volume at the end of the programming cycle.

neurons is modified based on neural activities in presynaptic and postsynaptic cells. Spike-timing dependent plasticity (STDP), a form of Hebbian learning, which relies on relative spike timings of presynaptic and postsynaptic neurons has been discovered in several biological systems[8−10] in 1990s. STDP as a quantifiable, robust phenomenon providing an intuitive cellular mechanism for learning has attracted a lot of attention in theoretical studies on the learning rules.[11−14]

CMOS based architectures[15−17] have been designed to emulate biological synapses in the past. However, this approach occupies a very large area (at least ∼10 transistors per synapse) and, hence it is not practical for designing massively parallel systems with 10^{15} of these circuits. Recently, several devices[18−20] have been demonstrated that could be potentially used to emulate biological synapses. In addition to basic synaptic functionality, an electronic analogue of a biological synapse[8−10] needs to exhibit STDP with a cumulative weight change dependent on the number of spike pairs and a maximum weight change of 100%. Such a device should also have programming flexibility to capture the variation and the different forms of STDP observed in biological synapses. A nanoscale electronic device with these characteristics that can operate on the picojoule energy consumption level is yet to be demonstrated. Motivated by this challenge, we investigate the use of phase change materials as electronic synapses by engineering their switching characteristics. Phase change materials have been intensively explored for memory applications due to its scalability, fast write/erase speed, and good endurance characteristics[21−26] and recently introduced in the marketplace as a commercially

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available product.[25−27] In this work, we capitalize on advances in this mature memory technology and engineer it for a completely different functionality, namely, implementation of synaptic plasticity for brain-inspired computing. Different from digital memory applications, here we utilize the continuous transition between resistance levels of phase change materials in an analog manner to emulate biological synapses (Figure 1a). We explore the important concepts such as implementation of STDP by gradual programming of phase change devices and modulation of STDP parameters and demonstrate low energy consumption of electronic synapses. Scalability of phase change devices down to the nanoscale[25] and the cross-point architecture stackable to three-dimensions (3D) offer the potential for reaching the ultrahigh density (10^{10} cm^{-2}) and compactness of brain while achieving low power consumption (∼1 pJ per synaptic event). Nanoscale electronic synapses can be integrated with neuromorphic neuron circuits[15] on a microchip (similar to the functional columns in the brain) which can process information autonomously in complex environments by learning, adaptation, and probabilistically associating information. Moreover, it can provide a new platform for real time brain simulations, which will allow new advances in the field of neuroscience.

Phase change materials exhibit a unique switching behavior between amorphous (high resistivity) and crystalline (low resistivity) states with the application of electric pulses that are large enough to generate the heat required for phase transformation. Chalcogenide glass, more specifically GST ($Ge_2Sb_2Te_5$), is one of the widely used materials for phase-change memory applications.[28] The device structure, used for synaptic application in this work, consists of a phase change material deposited between a bottom electrode with a small contact area and a top electrode (Figure 1, Supporting Information). Set and Reset states refer to the crystalline and amorphous phases, respectively. To investigate the feasibility of using phase change materials in nanoscale electronic synapses, devices with 75 nm bottom electrode diameter were fabricated. Details of device fabrication are given in the Supporting Information. Electronic threshold switching is observed in measured current−voltage characteristics of phase change devices fabricated with GST between a nanoscale W bottom electrode capped by TiN and a TiN top electrode (Figure 2, Supporting Information).

A continuous transition between intermediate resistance states is the first requirement to achieve the analog nature of synaptic weight change in biological synapses.[8] There have been several reports showing that intermediate resistance states can be programmed between the fully set and the fully reset states.[29−31] Cross-sectional transmission electron micrographs (TEM) of electronic synapses programmed to fully set, partially reset, and fully reset states are shown in Figure 1b. In the fully set state, the cell resistance is ∼500 Ω and the GST layer is polycrystalline everywhere in the cell, including the regions close to the TiN bottom electrode. The cross section TEM of the partially reset cell is taken after the cell is programmed to 200 kΩ by applying a low amplitude reset pulse. A small mushroom-shaped amorphous region is observed at the top of the bottom electrode. For the fully reset cell, the amorphous volume covers the entire bottom electrode region and the mushroom-shaped amorphous region is much larger after the application of a high amplitude reset pulse. The cell resistance is dominated by the high resistance of the amorphous GST region, which is measured as 2 MΩ for the fully reset state. The electron diffraction pattern in the bottom right panel (Figure 1b) indicates that GST away from the bottom electrode is in the crystalline state. The diffraction pattern (inset of the fully reset state in Figure 1b) of the mushroom-shaped region confirms that GST is in amorphous state close to bottom electrode for the fully reset state.

Conventional phase change materials for digital memory applications are programmed to intermediate resistance levels by current pulses. Those programming schemes provide up to 16 intermediate resistance levels. However, for synaptic applications very fine control of resistance, close to 1% change per synaptic activity, is required. Here, we use gradually increasing voltage pulses with a custom engineered timing to probe the intermediate resistance levels and to maintain continuous transitions between adjacent levels. An order of magnitude change in the phase change cell resistance was achieved through 100 steps for both the set and reset transitions. The repeatability of this gradual phenomenon was confirmed through many cycles as shown in Figure 1c. Gradual reset of the cell resistance is implemented by using pulses with increasing amplitude in the 2−4 V voltage range with 20 mV voltage steps. The pulse width and rise and fall times of the reset pulses are 75, 25, and 25 ns, respectively. Gradual set of the cell resistance is achieved by using stair-case pulses with an increasing step of 0.1 V. Each voltage value in the step is repeated continuously for 20 pulses, i.e., 20 pulses for each voltage 0.5, 0.6, 0.7, 0.8, and 0.9 V. The pulse width and rise and fall times of the set pulses are 5 μs, 500 ns, and 500 ns, respectively. To study the reliability of our current cells, we performed endurance measurements by repeatedly switching between two different states (max and min resistance). The cell resistance measured at different switching cycles is shown in Supplementary Figure 3 in the Supporting Information. The phase change cells used in this study show no degradation up to 10^7 cycles, while the endurance can be as high as 10^{12} cycles for high-quality devices fabricated on industrial standards.[21]

In order to understand and validate the gradual set/reset in GST cells, finite element simulations are performed using COMSOL.[32] Figure 1d shows the temperature distribution across the cell for gradually increasing voltage pulses. The region within the black borderline corresponds to the part of the phase change material that is heated above the melting temperature ($T > 900$ K) and hence would be amorphized at the end of the programming cycle resulting in higher cell resistance. The amorphous region grows gradually at the top of the nanoscale bottom electrode leading to numerous intermediate resistance states. More detailed information about simulations is provided in the Supporting Information.

STDP is interpreted as a learning rule that defines how a synapse participates in information processing and brain network functions. According to STDP learning rule, plasticity or so-called synaptic weight depends on the relative timing of pre- and postsynaptic spikes. The synapse potentiates (increase in synaptic weight or conductance) if presynaptic spike precedes postsynaptic spike repeatedly, and the synapse depresses (decrease in synaptic weight or conductance) if postsynaptic spike precedes presynaptic spike repeatedly (Figure 2a). The precise pre-/postspike timing window, which controls the sign and magnitude of synaptic weight modification, is around 100 ms for biological synapses.[8−10] STDP strengthens synapses that receive correlated input, which can lead to the formation of stimulus-selective columns and the development of selectivity maps in the brain.[11] A conventional version of a STDP circuit built with CMOS technology includes more than 20 transistors[16] which occupy a significantly larger area than a single element nanoelectronic synapse. As demonstrated in this work, a very fine control of intermediate resistance levels in a phase change material is

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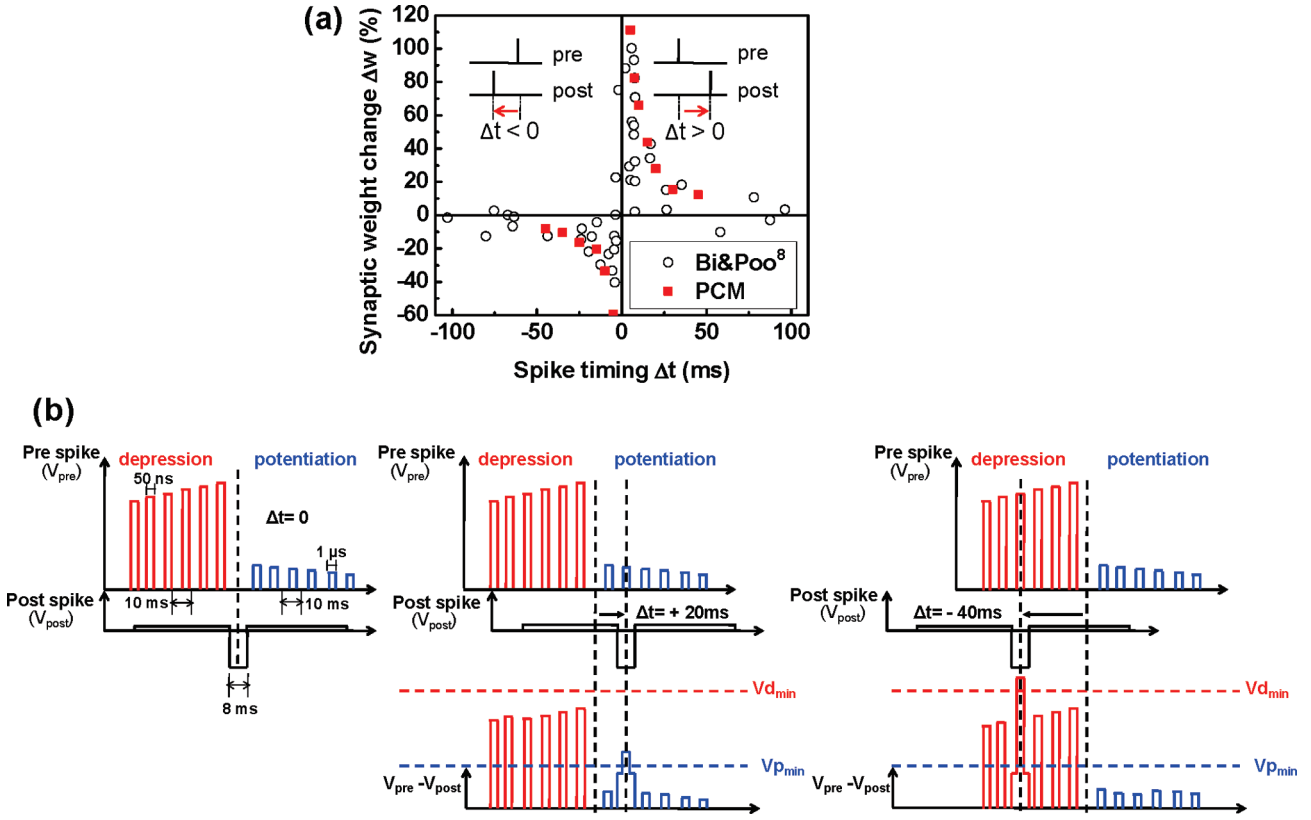

Figure 2. Implementation of spike-timing-dependent plasticity with PCM cells. (a) Synaptic weight change is plotted as a function of relative timing of pre- and postspikes. Measured STDP characteristics are shown along with the biological data measured in hippocampal glutamatergic synapses by Bi and Poo.[8] The percentage change is calculated with respect to same initial value for all Δt points. (b) The pulsing scheme used to implement STDP with PCM cells is shown. The schematic explains the net programming voltage applied across the electronic synapse at $\Delta t = 0$, $+20$ ms, and -40 ms. $V_{P_{min}}$ and $V_{d_{min}}$ are the minimum voltage amplitudes that can induce potentiation and depression across synapse, respectively.

required for the implementation of the neuromorphic learning rule, STDP. A phase change memory (PCM) cell serves as a nanoscale electronic synapse. In a neuromorphic design, the pre- and postspikes are generated by neuron circuits, which are interconnected by nanoscale electronic synapses. Here, the pre- and postspikes are generated by an arbitrary waveform generator, emulating the presynaptic and postsynaptic neuron circuits. The prespike is applied to one end (top electrode) of the electronic synapse (PCM) and the postspike is applied to the other end (bottom electrode). The shapes of pre- and postspikes are not same as the biological action potentials. They are developed based on the pulsing scheme used in gradual set/reset experiments with GST cells in order to induce desired STDP characteristics for the synapse. A simplified schematic with a fewer number of pulses than the STDP schemes used for the experimental data is illustrated in Figure 2b. Prespike is a pulse train, consisting of depression pulses with increasing amplitudes and potentiation pulses with decreasing amplitude. Depression and potentiation correspond to reset and set states, respectively. Total duration of prespike is 120 ms. The pulse width and rise and fall times of depression pulses are 50, 10, and 10 ns, respectively, while they are 1 μs, 100 ns, and 100 ns for potentiation pulses. The time spacing between two pulses is kept constant, 10 ms for this specific STDP scheme, and can be tuned to modulate STDP behavior as shown later in this paper. The postspike serves as a gating function for the prespike. It is a low amplitude, continuous pulse with 120 ms duration with a short negative amplitude pulse of 8 ms at the center. The difference between the prespike and the postspike ($V_{pre} - V_{post}$) defines the net programming voltage applied across the electronic synapse at each point in time. For the case where pre- and postneurons spike simultaneously ($\Delta t = 0$), the postspike does not overlap with the depression or potentiation pulses of the prespike. For instance, if a preneuron spikes 20 ms before the postneuron ($\Delta t = 20$ ms), the negative part of the postspike will overlap with the second potentiation pulse. The overall potential drop across the electronic synapse will be above the potentiation threshold ($V_{P_{min}}$), which will result in a 60% increase in synaptic weight. $V_{P_{min}}$ is the minimum voltage amplitude that can induce any potentation across the electronic synapses. However, if the postneuron spikes 40 ms before the preneuron ($\Delta t = -40$ ms), the negative part of the postspike will overlap with one of the low amplitude depression pulses and result in a -15% decrease in synaptic weight. Similarly, by repeating the spike scheme for different Δts in the -50 to 50 ms range, the overall STDP curve is obtained as shown in Figure 2a. Our measured STDP characteristics are in good agreement with the biological data measured in hippocampal glutamatergic synapses by Bi and Poo.[8]

Although biological synapses exhibit much complex behavior, the effect of STDP can be quantified by fitting the biological data using a simple exponential as in eq 1.

$$\Delta w = Ae^{-\Delta t/\tau} \quad (1)$$

where Δw is the percentage change in synaptic weight with respect to the initial value and Δt is the pre-/postspike interval. A

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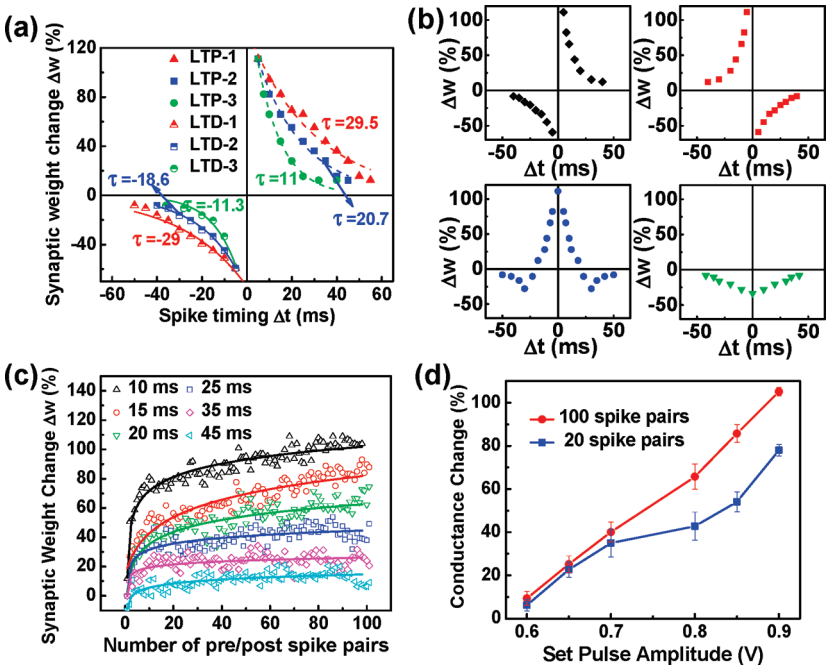

Figure 3. Modulation of STDP time constant and dependence on number of pre-/postspike pairs. (a) STDP is measured on PCM synapses by modifying the spacings and amplitudes of the pulses in the prespike. LTP1, LTP2, and LTP3 correspond to three different prespike configurations for long-term potentiation (LTP). LTD1, LTD2, and LTD3 correspond to three different prespike configurations for long-term depression (LTD). Time constants are modulated for the STDP curve with the spike timing delay in the range of 10−30 ms for potentiation and −10 to −30 ms for depression. (b) Different forms STDP learning rules. Upper left is asymmetric STDP with potentiation at positive Δt. Upper right is asymmetric STDP with potentiation at negative Δt. Lower left is symmetric STDP with potentiation at positive $\Delta t = \sim 0$. Lower right is symmetric STDP with depression at all Δt. (c) Synaptic weight change as a function of number of applied pre/postspike pairs is shown for different pre/postspike timings (Δt, from 10 to 45 ms). (d) The conductance change of GST cells is plotted as a function of set voltage amplitude for 10 and 100 spike pairs.

and τ are two free parameters found by fitting the data. A and τ correspond to the scaling factor and the time constant for STDP curve, respectively. These exponential fits are very convenient to formalize STDP into a simple parametric model to be used in computational studies. In recent years, biological experiments have shown that the time constant of the STDP window can show significant variation depending on the location of the synapses in the brain.[33−38] For instance hippocampal glutamatergic synapses show potentiation with τ of 16.8 ms while τ for visual cortex neurons is measured as 13.3 ms. It is commonly believed that synapses with different τ may serve specific functions in information processing at different stages of neural pathways. The electronic synapses capturing this variation in STDP characteristics of biological synapses can bring another degree of freedom for designing complex cognitive systems in the future. Control of τ can be achieved by modifying the amplitude and the time spacing between the individual pulses in the prespike. As shown in Figure 2b, the pulses in prespike are equally spaced and the pulse amplitude increases or decreases linearly. We can decrease the spacing between the pulses with the smallest spacing between the two highest amplitude depression and potentiation pulses. In doing so a sharper change in STDP characteristics and, hence, a smaller τ can be obtained. Moreover, an exponential increase and decrease in the amplitude of the depression and potentiation pulses can be implemented, respectively, instead of a linear increase and decrease in the pulse amplitude shown in Figure 2b. In order to show that we can control τ, STDP is measured on electronic synapses by modifying the time spacing and amplitude of the pulses in the prespike (Figure 3a). Time constants in the range of 10−30 ms for potentiation and −10 to −30 ms for depression are demonstrated. It is also possible to achieve higher τ values depending on the choice of spacing between pulses in the prespike.

Recent advances in neuroscience revealed that the synapses in the brain columns with different functionality can exhibit different forms of STDP.[37] The forms of STDP, that reflect the different information processing and storage needs depending on the particular neural circuit, have been accepted as kernels for modeling plasticity in several theoretical studies.[12,39,40] The role of different STDP forms is still an active research area in neuroscience. Recent work[41] has shown that the symmetric STDP (the lower left panel in Figure 3b) can enable robust sequence learning. The noise immunity of a particular column is strongly correlated with the long-term-depression window of STDP. The different forms of STDP can be implemented using the same single nanoscale electronic synapse by modulating the order of potentiation and depression pulses in the prespike. Four different forms of STDP, (1) asymmetric STDP with potentiation at positive Δt, (2) asymmetric STDP with depression at positive Δt, (3) symmetric STDP with potentiation around $\Delta t = 0$, (4) symmetric STDP with depression at all Δt, in good agreement with the biological data[37] are demonstrated. Implementation of different STDP kernels is a significant step toward transferring all the theoretical work on learning algorithms, structural plasticity, and noise immunity to a hardware design.

In a biological brain there is no single spike event. The neurons in the brain continuously spike in the form of pulse trains with varying frequencies and the total weight change due to individual

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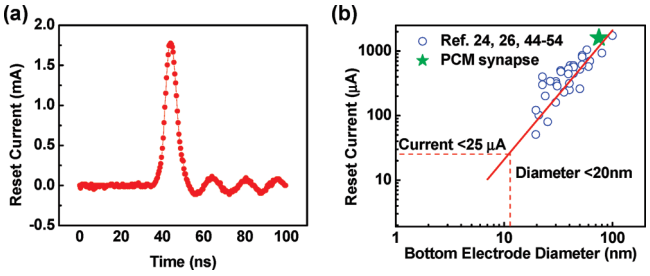

Figure 4. Energy and programming current analysis for PCM synapse. (a) Real time measurement of reset current flowing across the PCM synapse is shown. The reset pulse width is 10 ns and pulse amplitude is 5.5 V. The energy consumed during reset operation is $E = V \times I_{avg} \times t = 5.5\ V \times 0.9\ mA \times 10\ ns$, where $I_{avg} = I_{peak}/2$. (b) Literature data for reset current are shown as a function of equivalent contact diameter. The trend line is fitted for the linear scaling of the bottom electrode contact area as the device feature size goes down. The reset current for 20 nm contact diameter is estimated to be 25 μA. The reset current measured on PCM synapse is shown with the green star symbol.

spike pairs is cumulative. In most of the biological studies, about 60−100 pre-/postspike pairs are repeatedly applied for several minutes to induce long-term potentiation (LTP) or long-term depression (LTD). The repetition of pre-/postspike pairs result in a cumulative weight change dependent on the number of spike pairs with a maximum of 100%. The number of pairing events required to cause a certain amount of potentiation or depression during STDP shows variation depending on the type and location of synapses. For instance in the optic tectum of the tadpole in vivo, while a moderate amount of LTP was induced after 20 pre-/postspike pairs, maximum LTP was reached after 80−200 pre-/postspike pairs.[9] On the other hand, in the cortex, 15 or fewer pre-/postspike pairs were shown to induce a high level of LTP.[42] The required number of pre-/postspike pairs is a parameter that needs to be implemented to represent the probability of inducing potentiation in a neural circuit. In Figure 3c, synaptic weight change as a function of number of applied pre-/postspike pairs is shown for different pre-/postspike timings (Δt, from 10 to 45 ms), measured on the same electronic synapse. A sharp increase in the synaptic weight change in the first 10−20 spike pairs is followed by a slower increase and saturation close to the 100th spike pair. The measured dependence of STDP on number of pre-/postspike pairs for electronic synapses is very similar to the trend observed in some of the synapses in young rat visual cortex.[42] These results can be interpreted as the probability of inducing LTP in synapses depends on the number of the spike pair repetitions.

The dependence on number of pre-/postspike pairs for electronic synapses can be understood from a potentiation pulse amplitude point of view. A synaptic weight increase, which can be induced by a single pre-/postspike pair, can also be induced by a larger number of pre-/postspike pairs if the amplitude of potentiation pulses in STDP scheme is reduced. Lowering the potentiation (set) pulse amplitude results in a smaller fraction of crystalline region inside the amorphous cap in GST. The crystalline GST volume expands as more set pulses are applied repeatedly. The conductance change of GST cells, extracted from Figure 3c, is plotted as a function of set voltage amplitude for 20 and 100 spike pairs in Figure 3d. It can be seen that to achieve the same conductance change, the smaller amplitude spikes require a larger number of repetition pairs. This characteristic of the phase change materials allows for including the number of spike pairs as a parameter in cognitive system design while covering the required range measured in biological experiments.

Neuromorphic systems emulated by traditional CMOS circuits and MOS capacitors occupy significant area and have a substantial energy consumption of about $\sim 10^{-9}$ J per synaptic event.[43] In order to mimic the energy efficiency of biological systems, a more aggressive approach, that achieves energy consumption per operation in the order of a few picojoules, is needed. The energy consumption of our electronic synapses is calculated by measuring the current that flows across the phase change cell during pre-/postspiking events. Figure 4a shows real time oscilloscope trace of the current flowing across the synapse while being programmed with a 10 ns pulse width. The peak reset current is measured as 1.8 mA. The energy consumed to program the cell to reset state (depression) is determined as ~50 pJ ($E = V \times I_{avg} \times t = 5.5\ V \times 0.9\ mA \times 10\ ns$, where $I_{avg} = I_{peak}/2$), while the energy consumption for set operation (potentiation) is only 0.675 pJ ($E = V \times I_{avg} \times t = 0.9\ V \times 0.075\ mA \times 10\ ns$) as the cell current is much lower during set programming. The energy consumption in electronic synapses is dominated by the high reset current required to melt-quench the GST to its amorphous phase. The switching characteristics and the reset current have been intensively investigated for nonvolatile memory applications in the literature. Figure 4b shows the reset current reduction as a function of the equivalent bottom electrode diameter, with the data from recent publications.[24,26,44−54] The reset current scales with the effective bottom electrode area of the phase change memory cells and an average current density of $\sim 20 MA/cm^2$ is required to program the cells. The measured reset current of 1.8 mA for electronic synapses with 75 nm bottom electrode diameter agrees well with this scaling trend. The scaling trend line illustrates that reset currents as low as 25 μA will be sufficient for electronic synapses with a <20 nm bottom electrode diameter. The energy consumption for <20 nm electronic synapses is projected as 0.027 pJ and 2 pJ for set and reset operations, respectively. In addition to minimizing the size of electronic synapses with various sublithographic techniques, optimal structures to achieve better current localization and thermal isolation[54] can further reduce energy consumption to less than picojoule levels for electronic synapses made from phase change materials. A recent study[55] has shown that phase change memory devices fabricated with carbon nanotube electrodes can exhibit reset energy consumption as low as 100 fJ. It has also been demonstrated that switching from the amorphous to crystalline state can be achieved for phase change nanoparticle sizes as small as 1.8 nm[56] showing promise for future scaling of the cognitive systems.

In this work we have demonstrated a new single element nanoscale device, based on the successfully commercialized phase change material technology, emulating the functionality and the plasticity of biological synapses. The electronic synapse demonstrated here is an excellent analogue of biological synapses, implementing STDP with a cumulative weight change dependent on the number of spike pairs and a maximum weight change of 100%. To our knowledge, this is the first demonstration of a single element electronic synapse with the capability of both the modulation of the time constant and the realization of the different STDP kernels. The nanoscale size and picojoule level energy consumption are significant steps toward reaching the compactness and energy efficiency of a biological brain for future brain-inspired computational systems. Our work can be easily extended to a cross-point architecture allowing

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three-dimensional stacking of many layers of electronic synapses, thereby enabling us to approach the massive parallelism of the brain.

■ ASSOCIATED CONTENT

Supporting Information. Phase change synaptic device fabrication, basic electrical characterization of fabricated devices, measurement setup for implementation of synaptic plasticity, and details of finite element simulations for gradual resistance change. This material is available free of charge via the Internet at http://pubs.acs.org.

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